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Applied Physics Letters -- March 13, 1995 -- Volume 66, Issue 11, pp. 1388-1390

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Fabrication of nanometer-scale side-gated silicon field effect transistors with an atomic force microscope

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(Received 9 November 1994; accepted 18 January 1995)

The fabrication of nanometer-scale side-gated silicon field effect transistors using an atomic force microscope is reported. The probe tip was used to define nanometer-scale source, gate, and drain patterns by the local anodic oxidation of a passivated silicon (100) surface. These thin oxide patterns were used as etch masks for selective etching of the silicon to form the finished devices. Devices with critical features as small as 30 nm have been fabricated with this technique. ©1995 American Institute of Physics.

doi:10.1063/1.113210

PACS: 85.42.+m, 85.30.Tv, 85.40.Hp Additional Information

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